**CS2100 Midterm CheatSheet**

**C Language** (2s Complement is used!)

**~** is NOT, ^ is XOR (Bitwise Operator)

! is boolean operator, not bitwise operator

%lf is used when you want to scan double

\t is used in printing to print a tab

Range of int: -231 to 231 – 1

*Syntax of Structure*

typedef struct { Use . if you want to access

members….. members of a structure.

} <structure name>**;**

We may do assignments with structure, meaning if we assign one structure to another structure variable, it will copy all the members of the structure into the respective members of the structure of the structure variable.

(\*player\_ptr).name /\*legal\*/

\*player\_ptr.name /\*illegal as treated as \*(player\_ptr.name)/

player\_ptr->name /\*legal\*/

**Declaring an array of pointers:** type \*a[]

In ASCII table, it starts with **capital letter first** then lowercase letter. Each capital letter and it’s corresponding lowercase letter differs by a **decimal value of 32**

**Number System**

*Conversion from decimal to base-R*

Whole number: repeated division by R (copy resultant digits down to up)

Fractional number: repeated multiplication by R (copy resultant digits up to down)

*Negation of a number*

**1s**: -x = 2n – x – 1 (n is number of bits of x in binary)

To get negation of x: invert all the bits of x (same for fraction)

**2s**: -x = 2n – x (n is number of bits of x in binary)

To get negation of x: invert all the bits of x and **add 1**

(if fraction, same thing, but plus 1 at the **rightmost digit** after the “.”)

*Addition*

**2s:**Perform addition as usual, **ignore carry out of the MSB**, check for overflow (occur when the resultant sign bit is different from that of the operands in the case where both operands have the same sign)

1s: Same as above, **however** **if there is a carry out of the MSB, add 1 to the rightmost digit (**same in fractional num)

**Hexa: …, 9, A, B, C, D, E, F**

*Subtraction (a – b)*

Convert b to its complement and perform addition.

*Excess*

\*Binary rep. of x in excess-N = Binary rep. of (x + N)

\*Dec rep. of x represented in excess-N: Convert x back to decimal and minus the result by N

*IEE 754 Single-Precision Floating-Point Rep*

1-bit sign, 8-bit exponent represented in **EXCESS 127**, 23-bit mantissa   
**Decimal to IEE:** Convert the number to binary, normalize it, and fill in the parts accordingly

*Sign Extension*

***Unsigned****:* Copy all the bits and put it at the rightmost part, fill the unfilled front part with zeros

***Signed****:* Copy **the magnitude part** and put it to the rightmost part, copy sign bit and put it at the first bit, then fill the in -between gap with zeros

***1s and 2s***: Copy **all the bits** and put it at the rightmost part, fill the unfilled front part with the sign bit of the original num.

**MIPS** (Immediate is a **2s** **complement**)

Given k-bit addresses, you can have 2k addresses.

*Branching*

The immediate field is equal to the number of instructions you skip over, starting from **the end of the branch instruction**. (if jump backwards **then immediate is -ve**, must count the branch instruction as one of the instruction to skip too!)

If branch is not taken: PCnew = PC + 4

If branch is taken: PCnew = (PC + 4) + (immediate x 4)

*Jump*

Given address of instruction, drop the first 4 bits and the last 2 bits, the rest will be your immediate field.

Getting NOT from NOR: nor x, x, $zero (x is the same register)

Getting NOT from XOR: xor x, x, y (y is the register that contain all 1s)

ANDI, ORI, XORI will **zero extend** the 16-bit immediate **to the left**!

LB and LH will **sign extend** the 8 bits and 16 bits that they fetched respectively from the memory and store it in the register

SB and SH will only store the 8 and 16 **least significant bits** in the register mentioned respectively into the memory

LUI shifts the given 16 bit immediate to the left by 16 bits and concatenate it with 16 zeros.

To generate a mask (i.e. keep the bits you want) using ANDI, you use bit 1 to keep the bit that you want and 0 for the bit you don’t want.

OR can be used to force certain bits to become 1.

**ISA** (MSB = most significant Byte)

Big-endian: MSB are stored in lower addresses

Little-endian: LSB are stored in lower addresses

**Data Path**

**Instruction Execution Cycle:** Fetch, Decode, Operand Fetch, Execute, Result Write (Store)

**Multiplexer**: Inputs: n lines, Control: m bits where n = 2m

**Control** (Note the following control signals aren’t complete)

**RegDst**: 0 -> choose rt; 1-> choose rd

**ALUSrc**: 0 -> choose RD2; 1-> choose SignExt(Inst[15:0])

**MemToReg:** 0 -> choose ALU result; 1-> choose Memory Read Data

**PCSrc**: 0 -> PC + 4; 1 -> (PC+4) + SignExt(Inst[15:0]) << 2

***ALU Control***

0000 AND | 0001 OR | 0010 add | 0110 subtract | 0111 slt

1100 NOR

**ALUOp**

00 lw/sw | 01 beq | 10 R-Type

**Power of 2**

27 = 128, 28 = 256, 29 = 512, 231 = 2147483648

**Boolean Algebra**

A + A’ = 1 A.A’ = 0 (Complement / Inverse)

X + X = X X.X = X (Idempotency)

(X’)’ = X (Involution law)

X + X.Y = X X.(X+Y) = X (Absorption)

X + X’.Y = X + Y X.(X’+Y) = X.Y (Absorption(variant))

X.Y + X’.Z + Y.Z = X.Y + X’.Z (Consensus)

(X+Y).(X’+Z).(Y+Z) = (X+Y).(X’+Z) (Consensus)

A.B’ + A’.B = AB

A.B + A’.B’ = (AB)’ or AB

**Kmaps**

**A drawing of a person

Description automatically generated A close up of a logo

Description automatically generated**

**A screenshot of a cell phone

Description automatically generated**

**Delay** in Sum and Carry of a **n-bit parallel adder**

S = 2nt

C = (2n + 1)t // Maximum delay of the parallel adder

**Decoder**

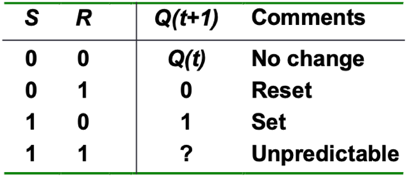
The order of the outputs corresponds to the order of the **minterms**

**Sequential Circuit (Characteristic Table)**

**S-R flip flop D-flip flop**

A drawing of a person

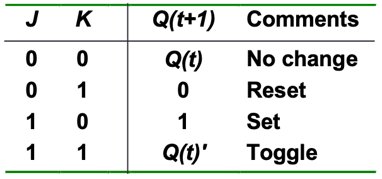
Description automatically generatedQ(t + 1) = S + R’.QQ(t + 1) = D

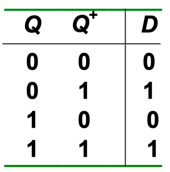


**J-K flip flop** **T flip-flop**

Q(t + 1) = J.Q’ + K’.Q Q(t) = T.Q’ + T’.Q

A screenshot of a cell phone

Description automatically generated

**Excitation Table**

**A drawing of a person

Description automatically generated**

**A drawing of a person

Description automatically generated**A picture containing text

Description automatically generated

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**Pipelining (Instructions Execution Time)**

**Single-cycle:** **I x Tsingle cycle** Tsingle cycle =

**Multiple-cycle:** **I x Average CPI x CTmulti**

CTmulti = max(Tstage), CPI = num of cycles per instruction

**Pipeline: Numcycles x CTpipeline = (I + N – 1) x (max(Tstage) + Td)**

N = num of stages in pipeline (MIPS is 5)

Td = pipeline overhead

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**Early Branching:** If no early branching (i.e. **decide** in MEM), then need to **delay** **3 cycles** (refer top right corner!)

If early branching (i.e. **decide** in ID), **delay** **1 cycle**)(But this depends on the register involved in the comparison!)

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**Cache**

**Average Memory Access Time**

(Hit rate x Hit Time) + [(1 – Hit rate) \* Miss Penalty]

1 KB = 210 byes =1024 bytes, 1 MB = 220 bytes, 1 GB = 230 byes

**Direct Map** Given block size = 2M, num of blocks in cache = 2N

**Block Index** = Block number % num of blocks in cache

**Mapping :** Offset = M bits, Block Index = N bits

Tag = 32 – N – M bits

**N-way Set associative**

**Set Index** = Block number % number of **sets** in cache

**Mapping:** Offset = M bits, **Set** index = N bits

Tag = 32 – N – M bits {num sets in cache = 2N}

**Fully Associative:** Offset = M bits**,** Tag = 32 – M bits

**Writing Policies**

**Write Through:** Write into **cache & memory** (Write into cache & write buffer, memory controller will write into memory from write buffer.

**Write Back:** Write into the **cache only** and only write into the memory if the block is evicted (**and updated**, by **using dirty bit** to indicate: 0 if not updated, 1 if updated)

**Write MISS Policies**

**Write Allocate:** Load the entire block into the cache, write only the word that is changed. Writing back to the memory depends on writing policies.

**Write Around:** Only write directly into the memory. Do not load the entire block into the cache.